IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of: **Linden Minnick**

Group Art Unit: **2151**

Application No.: **10/007,082**

Examiner: **Madamba, Gleneford J.**

Filed: **12/06/2001**

For: **METHOD AND APPARATUS FOR PROCESSING LATENCY SENSITIVE ELECTRONIC DATA WITH INTERRUPT MODERATION**

APPEAL BRIEF
IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This brief is in furtherance of the Notice of Appeal, filed in the above-captioned case on July 30, 2008. Applicants (hereafter "Appellants") hereby submit this Brief (37 C.F.R. § 41.37). The fees required under § 41.20(b)(2), and any required petition for extension of time for filing this brief and fees therefore, are dealt with in the accompanying Transmittal of Appeal Brief. Appellants respectfully request consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above-captioned patent application. An oral hearing is not desired.

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This brief contains these items under the following headings, and in the order set forth below (37 C.F.R. § 41.37c(1)):

Page 14 of this brief bears the practitioner's signature.

I. REAL PARTY IN INTEREST (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest in this appeal is Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California, 95052, to whom the invention is assigned.

II. RELATED APPEALS AND INTERFERENCES (37 C F R § 41.37(c)(1)(ii))

With respect to other appeals or interferences that will directly affect, or be affected by, or have a bearing on the Board's decision in this appeal, to the best of Appellant's knowledge, there are no such appeals or interferences.

III. STATUS OF THE CLAIMS (37 C F R § 4137(c)(1)(iii))

The status of the claims in this application are:

A. TOTAL NUMBER OF CLAIMS IN APPLICATION Claims 1-31 are currently pending in the application.

B. STATUS OF ALL THE CLAIMS

1. Claims cancelled: none.
2. Claims withdrawn from consideration but not cancelled: NONE.
3. Claims pending: 1-31.
4. Claims allowed: NONE.
5. Claims rejected: 1-31.

C. CLAIMS ON APPEAL

Claims 21-35 are on appeal.

IV. STATUS OF AMENDMENTS (37 C.F.R. § 41.37(c)(1)(iv))

A response was not submitted in response to the Final Office Action mailed on February 01, 2008. A response was submitted on 10/18/07 in response to the Office Action mailed 5/18/07. The response included amendments to the claims. The amendments were entered. A copy of all claims on appeal is attached hereto as an appendix of claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER (37 C.F.R. * 41.37(c)(1)(v))

There are four independent claims: 1, 11, 20 and 29. Independent claim 1 pertains to an input/output (I/O) device. (See, e.g., Fig. 1, ¶0012, ¶0018). The device is operative to receive a fragment of electronic data from a node on a network. (See, e.g., ¶ 0014). It determines characteristics of the fragment of electronic data, e.g., using a parsing module. (See, e.g., Fig. 1 and ¶0018). The I/O device moderates one or more interrupts to a processor (e.g., using an interrupt management module) if the characteristics of the fragment of electronic data indicate that the fragment of electronic data is latency-sensitive data. (See, e.g., Fig. 1 and ¶¶0015, 0018).

Independent claim 11 pertains to a method of moderating one or more interrupts of an associated computing platform. The method comprises receiving a fragment of electronic data from a node on a network. (See, e.g., ¶ 0014). It includes determining characteristics of the fragment of electronic data. (See, e.g., Fig. 1 and ¶0018). It includes moderating one or more interrupts to a processor if the characteristics of the fragment of electronic data indicate that the fragment of electronic data is latency-sensitive data. (See, e.g., Fig. 1 and ¶¶0015, 0018).

Claim 20 pertains to a storage medium having stored thereon instructions, that when executed by a computing platform, result in execution of a method of processing latency sensitive electronic data. (See, e.g., original claim 20). The method comprises receiving a fragment of electronic data from a node on a network. (See, e.g., ¶ 0014). The method includes determining characteristics of the fragment of electronic data. (See, e.g., Fig. 1 and ¶0018). The method includes moderating one or more interrupts to the processor if the characteristics of the

fragment of electronic data indicate that the fragment of electronic data is latency-sensitive data. (See, e.g., Fig. 1 and ¶¶0015, 0018).

Claim 29 pertains to an input-output (I/O) apparatus. (See, e.g., Fig. 1, ¶0012, ¶0018). It receives a fragment of electronic data from a node on a network. (See, e.g., ¶ 0014). it determines characteristics of the fragment of electronic data. (See, e.g., Fig. 1 and ¶0018). It moderates one or more interrupts to a processor if the characteristics of the fragment of electronic data indicate that the fragment of electronic data is latency-sensitive data. (See, e.g., Fig. 1 and ¶¶0015, 0018).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. § 41.37(c)(1)(vi))

A. Claims 1, 3, 5, 11, 20 and 29 are rejected under 35 U.S.C 103(a) as being unpatentable over Johnson, U.S. Patent 5,905,874 in view of Duda et al (hereinafter Duda), U.S. Patent Number 7,065,762 131.

B. Claims 2, 4, 12, 13, 21, 22, 30, 31 are rejected under 35 U.S.C 103(a) as being unpatentable over Johnson in view of Duda and in further view of Drottar et al (hereinafter Drottar), Patent Number 6,333,929.

C. Claims 6-10, 15-19, 24-28 are rejected under 35 U.S.C 103(a) as being unpatentable over Johnson in view of Duda and in further view of Gentry Jr., Patent Number 6,434,651.

VII. ARGUMENT (37 C.F.R. § 41.37(c)(1)(vii))

A. REJECTION OF CLAIMS 1, 3, 5, 11, 20, and 29 UNDER 35 U.S.C. § 103

GROUP I: CLAIMS 1, 3, 5, 11, 20, and 29

All of the Independent claims in this Group, as well as the Application (claims 1, 11, 20, and 29) include the limitation: "moderate one or more interrupts to a processor if the characteristics of the fragment of electronic data [from a network node] indicate that the fragment of electronic data is latency-sensitive data."

Thus, all of the claims in the application are rejected under 103 based in whole or in part on Johnson combined with Duda. Johnson discloses an I/O device, (NIC) that is directed to improving data transfer latency. But it does not teach using interrupts in any way to achieve this objective. Rather, it teaches initiating writing network received data into the computer's memory (from the interface buffer) without waiting for the data to be completely loaded into the buffer. (See Johnson at col. 3, ll. 42-58). As recognized by the Examiner, nowhere does it teach moderating interrupts to a processor based on a characterization that received data fragments (packets) are latency sensitive. As discussed in the following paragraph, Duda does not provide this missing feature and for this reason alone, the two references cannot render Applicant's claims unpatentable because alone or in combination, they do not teach every claimed element.

Acknowledging that Johnson fails to teach this feature, the Examiner asserts, in the response to Applicant's arguments, that Duda discloses this feature as follows:

> For example, and with reference to Figures 2a-b and Figure 3, Duda expressly discloses "moderating interrupts to a processor based on the characterization that received data fragments are latency sensitive.

(Office Action at pages 4 and 5). This is factually not correct. Duda does not teach moderating interrupts *based* on the characterization that received data fragments are latency sensitive. Rather, Duda discloses a network switch that examines the contents of received data packets and determines an appropriate queue based on that content (for example, latency sensitivity). (See Duda at Col. 5. at ll. 2++ regarding Figure 2A). Duda goes on to describe its preemptive scheduling process, which in response to an interrupt, implements the content-based queuing among other things. (See Duda at Col. 5, l. 56 to Col. 6, l. 18). This portion of Duda is cited by the Examiner as support for support that Duda teaches interrupt driving based on its content based fragment characterization. But this is the eact opposite of what Duda teaches. Duda teaches content based queuing that is initiated in response to interrupts, the opposite of moderating (or controlling) interrupts based on or in response to packet data content (whether a fragment is latency sensitive).

Thus, the cited references do not teach this feature, as asserted by the Examiner, and the 103 rejections should be reversed.

Furthermore, the references give no incentive or motivation to modify either reference to include the feature. In fact, Johnson actually teaches away from its being modified in the way proposed by the Examiner to fulfill this feature. It states that memory mapped schemes, which use interrupts to invoke the host processor to service network interface data transfer tasks, are

less desirable than direct memory access (DMA) methods because they involve inefficiency and require valuable host processor resources. (See Johnson at col. 7, l. 60 to col. 8, l.). In other words, Johnson counsels against using interrupts to involve the processor in servicing a NIC data transfer task. Thus, based on these teachings, one would certainly not look for or consider any kind of an interrupt based solution for improving latency or otherwise modifying Johnson in this way. Therefore, the references should not be combined or modified, as urged by the Examiner.

B. REJECTION OF CLAIMS 2, 4, 12, 13, 21, 22, 30, 31 UNDER 35 U.S.C 103(a)

GROUP II: Claims 2, 4, 12, 13, 21, 22, 30, 31

Claims 2, 4, 12, 13, 21, 22, 30, 31 are rejected under 35 U.S.C 103(a) as being unpatentable over Johnson in view of Duda and in further view of Drottar et al (hereinafter Drottar), Patent Number 6,333,929. Applicants stand and rely on its arguments above as to why Johnson and Duda do not combine to teach all of the claimed elements and furthermore, cannot be combined.

C. REJECTION OF CLAIMS 6-10, 15-19, 24-28 UNDER 35 U.S.C 103(a)

GROUP III: Claims 6-10,15-19, 24-28

Claims 6-10, 15-19, 24-28 are rejected under 35 U.S.C 103(a) as being unpatentable over Johnson in view of Duda and in further view of Gentry Jr., Patent Number 6,434,651.

Applicants stand and rely on its arguments above as to why Johnson and Duda do not combine to teach all of the claimed elements and furthermore, cannot be combined.

CONCLUSION

Based on the foregoing, Appellants request that the Board overturn the rejection of all pending claims and hold that all of the claims of the present application are allowable.

Appellants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Respectfully submitted,

Date: March 2, 2009

/Erik Nordstrom, Reg. No. 39,792/

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VIII. CLAIMS APPENDIX (37 C.F.R. § 41.37(c)(1)(viii))

The text of the claims involved in the appeal are:

1. (Previously Presented) An apparatus comprising:

an input/output (I/O) device operative to:
receive a fragment of electronic data from a node on a network;
determine characteristics of the fragment of electronic data;
moderate one or more interrupts to a processor if the characteristics of the fragment of electronic data indicate that the fragment of electronic data is latency-sensitive data.

2. (Previously Presented) The apparatus of claim 1, wherein the latency-sensitive data comprises an acknowledgement (ACK).

3. (Original) The apparatus of claim 1, wherein said I/O device comprises a network interface card (NIC).

4. (Previously Presented) The apparatus of claim 1, wherein the latency-sensitive data comprises one or more data packets that have a priority designation.

5. (Previously Presented) The apparatus of claim 1, wherein said I/O device is operative to moderate by substantially immediately asserting said one or more interrupts of said associated computing platform processor.

6. (Previously Presented) The apparatus of claim 1, wherein said I/O device is operative to moderate by deferring said one or more interrupts of said associated computing platform processor so that a predetermined number of interrupts per unit of time is not exceeded.

7. (Previously Presented) The apparatus of claim 1, wherein said I/O device is operative to moderate by deferring said one or more interrupts until a particular number of fragments of electronic data of a particular type are received by said I/O device.

8. (Previously Presented) The apparatus of claim 1, wherein said I/O device is operative to moderate by deferring said one or more interrupts until a particular quantity of electronic data is received.

9. (Original) The apparatus of claim 1, wherein said moderation of associated computing platform interrupt scheme is configurable through a user interface.

10. (Previously Presented) The apparatus of claim 1, further comprising:
said I/O device further being operative to measure a particular period of time after the receipt of a fragment of electronic data, and to moderate one or more interrupts of an associated computing platform after said particular period of time has elapsed.

11. (Previously Presented) A method of moderating one or more interrupts of an associated computing platform comprising:

receiving a fragment of electronic data from a node on a network;

determining characteristics of the fragment of electronic data;

moderating one or more interrupts to a processor if the characteristics of the fragment of electronic data indicate that the fragment of electronic data is latency-sensitive data.

12. (Previously Presented) The method of claim 11, wherein said latency-sensitive data comprises an acknowledgement (ACK).

13. (Previously Presented) The method of claim 11, wherein said latency-sensitive data comprises one or more data packets that have a priority designation.

14. (Original) The method of claim 11, wherein said moderating comprises substantially immediately interrupting said associated computing platform processor.

15. (Original) The method of claim 11, wherein said moderating comprises deferring said one or more interrupts of said associated computing platform processor if a predetermined number of interrupts per unit time is met or exceeded.

16. (Original) The method of claim 11, wherein said moderating comprises deferring said one or more interrupts until a particular number of fragments of electronic data of a particular type are received.

17. (Original) The method of claim 11, wherein said moderating comprises deferring said one or more interrupts until a particular quantity of electronic data is received.

18. (Original) The method of claim 11, wherein said moderating is configurable through a user interface.

19. (Original) The method of claim 11, and further comprising:
measuring a particular period of time after the receipt of a fragment of electronic data; and performing said moderating after said particular period of time has elapsed.

20. (Previously Presented) An article comprising:

a storage medium; said storage medium having stored thereon instructions, that when executed by a computing platform, result in execution of a method of processing latency sensitive electronic data comprising:

receiving a fragment of electronic data from a node on a network;
determining characteristics of the fragment of electronic data;
moderating one or more interrupts to a processor if the characteristics of the fragment of electronic data indicate that the fragment of electronic data is latency-sensitive data.

21. (Previously Presented) The article of claim 20, wherein said latency-sensitive data comprises an acknowledgement (ACK).

22. (Previously Presented) The article of claim 20, wherein said latency-sensitive data comprises one or more data packets that have a priority designation.

23. (Original) The article of claim 20, wherein said moderating comprises substantially immediately interrupting said associated computing platform processor.

24. (Original) The article of claim 20, wherein said moderating comprises deferring said interrupting of said associated computing platform processor.

25. (Original) The article of claim 20, wherein said moderating comprises deferring said one or more interrupts until a particular number of fragments of electronic data of a particular type are received.

26. (Original) The article of claim 20, wherein said moderating comprises deferring said one or more interrupts until a particular quantity of electronic data is received.

27. (Original) The article of claim 20, wherein said moderating is configurable through a user interface.

28. (Original) The article of claim 20, and further comprising:
measuring a particular period of time after the receipt of a fragment of electronic data; and
performing said moderating after said particular period of time has elapsed.

29. (Previously Presented) An apparatus comprising:

an input-output (I/O) being operative to:

receive a fragment of electronic data from a node on a network;

determine characteristics of the fragment of electronic data;

moderate one or more interrupts to a processor if the characteristics of the fragment of electronic data indicate that the fragment of electronic data is latency-sensitive data.

30. (Previously Presented) The apparatus of claim 29, wherein one of the one or more characteristics of the fragment of electronic data comprises packet type.

31. (Previously Presented) The apparatus of claim 30, wherein said packet type comprises an ACK (acknowledgement) packet.

IX. EVIDENCE APPENDIX (37 C.F.R. § 41.37(c)(1)(ix))

To the best of Appellant's knowledge, no evidence has been submitted pursuant to 37 CFR Sections 1.130, 1.131, or 1.132.

X. RELATED PROCEEDINGS APPENDIX (37 C.F.R. § 41.37(c)(1)(x))

(To the best of Appellant's knowledge, there are no related appeals or interferences.)